ABSTRACT

The present invention provides a sense circuit for DRAM memory cell to cover the events that a sense time becomes remarkably longer when a power source voltage is lowered, a sense time under the low voltage condition becomes shorter when temperature rises and a sense time changes to a large extent for fluctuation of processes. The present invention provides the following typical effects. A switch means is provided between the bit line BL and local bit line LBL connected to the memory cells for isolation and coupling of these bit lines. The bit line BL is precharged to the voltage of VDL/2, while the local bit line LBL is precharged to the voltage of VDL. The VDL is the maximum amplitude voltage of the bit line BL. A sense amplifier SA comprises a first circuit including a differential MOS pair having the gate connected to the bit line BL and a second circuit connected to the local bit line LBL for full amplitude amplification and for holding the data. When the bit line BL and local bit line LBL are capacitance-coupled via a capacitor, it is recommended to use a latch type sense amplifier SA connected to the local bit line LBL.